



For more information, contact:

Soitec Contact:

Camille Darnaud-Dufour
Vice President, Communications
Soitec
Mobile (U.S.): +1-650-796-0634
Mobile (France): +33-06-79-49-51-43
E-mail: camille.darnaud-dufour@soitec.com

Agency Contact:

Brandy Lee
MCA
Tel: +1-650-968-8900, ext. 129
E-mail: blee@mcapr.com

ASM Contact:

Willem Vermeulen
Director Central Marketing
ASM International N.V.
Tel: +31-30-2298411
E-mail: willem.vermeulen@asm.com

Investor Relations Contact:

MaryJo Dieckhaus
Investor Relations
ASM
Tel: +1-212-986-2900
E-mail: maryjo.dieckhaus@asm.com

FOR IMMEDIATE RELEASE

**SOITEC AND ASM INTERNATIONAL REPORT MAJOR BREAKTHROUGH IN
STRAINED SILICON-ON-INSULATOR DEVELOPMENT PROGRAM**

Soitec ramps industry's first 300-mm sSOI pilot line for product sampling

BERNIN, France, and BILTHOVEN, The Netherlands—July 12, 2004—Soitec (Euronext Paris) and ASM International N.V. (NASDAQ: ASMI; Euronext Amsterdam: ASM) today announced a major breakthrough in their joint development effort to combine the compelling speed/performance benefits of strained silicon with the power/performance benefits of silicon-on-insulator (SOI) technology. Key to this effort was successfully introducing a “wafer-level” strain—a capability of avid interest to the IC industry, as it will extend the technology advantages well beyond the highly publicized “local strain” in use today. The resulting new genre of strained SOI (sSOI) substrates that Soitec will bring to market is design independent and therefore expected to enable an entirely new generation of leading-edge integrated circuits (ICs).

Company officials report that the yearlong collaborative effort Soitec launched with ASM has resulted in strained SOI substrates that have an extremely high-quality, wafer-level strain without the elevated level of crystal defects that have traditionally plagued this process. The unprecedented quality of the strained layer reduced the defectivity levels to between 100 and 1000 times lower than the industry standard, bringing the sSOI quality close to that of standard SOI and bulk silicon.

As a result, chipmakers will have access to strained SOI substrates that promise to break through today's looming barriers of power dissipation—an increasingly critical roadblock to higher-performing chips. And, since wafer-level strain is now no longer dependent on IC design, sSOI substrates will enable a wider range of high-speed, low-power IC applications, including those with high-performance logic cores.

SOITEC AND ASM REPORT MAJOR BREAKTHROUGH IN STRAINED SOI PROGRAM....Page 2 of 3

“By successfully creating the industry’s first high-quality, wafer-level strained SOI technology, we have reached an important milestone in accelerating industry availability of sSOI silicon wafers and, ultimately, the future-generation chips these substrates will enable,” said André Auberton-Hervé, Soitec president and CEO. “In addition to being the first company to offer 300-mm sSOI wafers to the industry, Soitec’s roadmap calls for the first ramp of industrial-level quantities of these wafers. Consistent with our stated commitment to innovate, develop and industrialize next-generation engineered substrates, these 300-mm strained SOI wafers will help the IC industry overcome its performance barriers and enable the continued progression of Moore’s Law.”

Both Soitec and ASM have expressed their satisfaction at the successful development effort, which integrated state-of-the-art strained silicon technology, enabled by ASM, with Soitec’s industry-leading SOI technology. This was made possible by Soitec’s patented Smart Cut™ technology, which will be the key to high-volume production of sSOI devices. Soitec has been sampling 200-mm sSOI since Q2 ‘03, and is currently upgrading its 300-mm sSOI production line—the first of its kind worldwide—for sampling and pilot manufacturing. This early sSOI sampling enables the IC industry to explore this important path for improving device performance and meeting the emerging needs of the 65-nm technology node and beyond.

Arthur del Prado, ASM President and CEO, stated, “We are very pleased that our collaboration with Soitec has been so effectively synergistic in this important area of developing entirely new materials and sources of supply for the advanced CMOS industry. We were able to meet Soitec’s technical, quality and cost-of-ownership standards in a very short development period.”

To further support Soitec’s goals, earlier this year, ASM delivered a low-temperature-enhanced, 300-mm Epsilon® 3200 reactor to complement the 300-mm A412 vertical furnace already in use at Soitec’s 300-mm Bernin production facility. Both these ASM products were used during the joint development effort and have already been production proven at major factories around the world.

Overcoming sSOI Challenges

The benefits afforded by wafer-level strained SOI are highly desired by the IC industry. However, a major concern about the manufacturability of this technology has been its high level of crystal defects in the wafer-level strained silicon layer—typically resulting from the epitaxial technique used to grow the silicon germanium templates that produce the strain on the silicon layers. The power of Smart Cut technology is that the target high-quality epitaxial strained layer is split from the underlying high-defectivity epitaxial template and transferred to a host silicon wafer to form sSOI.

Commenting on the two companies’ efforts to overcome this challenge, Dr. Carlos Mazure, Soitec’s chief technology officer, noted, “The fast-paced and effective work by both companies has resulted in strained epitaxial material of unprecedented quality for such complex technology. Coupled with Smart Cut technology, this material represents a major step in the continued progress toward sSOI industrialization. This ability to innovate and improve the standards of the strained silicon epitaxial process is expected to lead to a broad portfolio of sSOI products. Our customer and internal evaluations show that the strain of sSOI is very robust, surviving the typical thermal budgets of 65-nm CMOS processes.”

-more-

About Soitec:

Soitec is the world's leading innovator and provider of the engineered substrates that serve as the foundation for today's most advanced electronic products. Headquartered in Bernin, France, the company's comprehensive portfolio of engineered substrates, including SOI and strained SOI, is manufactured using Soitec's proprietary Smart Cut™ technology—the defacto industry standard. With its strong global presence, patented technology and industry-leading production capacity, Soitec is helping to drive the performance and power advantages that are key to the smaller, more power efficient, and increasingly mobile electronic products favored by consumers worldwide. Soitec's shares and convertible bonds are listed on the Nouveau Marché of Euronext Paris (respectively ISIN code FR0004025062 – SOI and FR0000182537). For more information, visit the company's website located at www.soitec.com

About ASM International:

ASM International N.V. is headquartered in Bilthoven, the Netherlands. ASM International is a global company, serving one of the most important and demanding industries in the world. The Company possesses a strong technological base, state-of-the-art manufacturing facilities, a competent and qualified workforce and a highly trained, strategically distributed support network. ASM International's subsidiaries design and manufacture equipment and materials used to produce semiconductor devices. ASM International and its subsidiaries provide production solutions for wafer processing, assembly and packaging through their facilities in the United States, Europe, Japan and Asia. ASM International's common stock shares trade on NASDAQ (symbol ASMI) and the Euronext Stock Exchange in Amsterdam (symbol ASM). For more information, visit ASM's Web site at <http://www.asm.com>

Safe Harbor Statement under the U.S. Private Securities Litigation Reform Act of 1995: The statements regarding orders, earnings development and the effects of research and new products on ASM's future, and other matters discussed in this statement, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to economic conditions in the semiconductor industry, currency fluctuations, the timing of significant orders, market acceptance of new products, competitive factors, risk factors related to litigation and other risks indicated in filings from time to time with the SEC and Stock Exchange Authorities.

###

Editors' Note: SOI material, which incorporates a layer of silicon on an embedded layer of silicon dioxide, enables SOI-based chips to function at significantly higher speeds while reducing electrical losses—enabling a 2- to 3x-reduction in power consumption and a 20- to 30-percent improvement in device speed. In the newer strained silicon, electrons experience less resistance and flow faster, resulting in a 20- to 30-percent increase in transistor performance. Combining these technologies, in the form of strained SOI material, will enable chipmakers to realize the cumulative benefits of both technologies, permitting significant advances in device speed, power consumption and IC packing density. As a result, chipmakers will be able to bring faster, more power-efficient chips to market, while assuring SOI-based technology continuity.

Smart Cut and UNIBOND are trademarks of S.O.I. TEC Silicon On Insulator Technologies. ASM, Epsilon and Advance are registered trademarks of ASM International.